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Embedded Planet, LLC (3Jan00)

RPX Lite Programmer's/FW Manual - For Rev CW boards

Programming and FW Requirements for the RPXL

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Table of Contents

I. Overview 4
II. Chip Select Mapping 5
III. BSP Code Location 6
IV. Board Status and Control Registers (BSCRs) 8
V. I2C Devices/Addressing 11
A. SEP Format/Interface Structure 11
B. STTM Format/Interface Structure 12
C. System Integration Timers 13
D. PCMCIA Control Registers 13
E. Option Register Mask Table 14
VI. Interrupt Structure 15
VII. Processor Pin Assignments 16
A. Bus Interface Pins 16
B. PCMCIA Interface Pins 17
C. I/O Port Interface Pins 18
VIII. Performance 19
A. @ 20 or 25MHZ 19
B. @ 33MHZ 19

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C. @ 40MHZ 19
D. @ 50MHZ 19
E. @ 66MHZ 20
F. @ 81MHZ 20

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List of Tables

Overview of FW Related Functions 4
Chip Select Mapping 5
Code Location in x32 FLASH 6
BCSR0 8
BCSR1 9
BCSR2 10
BCSR3 10
I2C Address Map 11
TBSCR, RTCSC, and PISCR 13
PGCRA and PGCRB 13
OR Mask 14
Interrupt Structure for the RPX Lite 15
Bus Interface - Multiple Function Pins 16
PCMCIA - Multiple Function Pins 17

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I. Overview

The RPX Lite is a highly integrated SBC based on the Motorola MPC850 and MPC823. The MPC850 versions are targeted for the tel-com industries, while the MPC823 version is targeted for the industrial controls market.

Support is available for several commonly used RTOSs.

The functions included on the RPX Lite that are related to FW are listed as follows:

Table 1: Overview of FW Related Functions

Entity	Function
Processor	MPC850 (SR, DC, DH, etc.) or MPC823
DRAM	4MB or 16MB
FLASH	2MB, 4MB, 8MB, or 16MB
NVRAM	0KB, 32KB, 128KB, 512KB
10Base-T Ethernet	SCC2
Monitor Port	SMC1
Serial EEPROM	I2C
Serial Temp & Thermal Monitor	I2C
BCSR	BCSR0, 1, 2, and 3

The PCMCIA Port and the USB Port are supported in hardware, but it is the responsibility of the end user to develop the driver/application required for any given PCMCIA card or USB peripheral. Support for some PCMCIA Cards, such as ATA, will occur at a later date. A future release of the RPX Utility Program will support testing of the PCMCIA and USB hardware.

Expansion Boards will be supported as they are designed (T1/E1, xDSL, Video, etc.)

For Hardware Setup information, see the RPX Lite User's Manual

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II. Chip Select Mapping

Table 2: Chip Select Mapping

Chip Select Number	Port Size	Function/ Address	Comment
CS0#	x32	FLASH (x32) FE00	Reset Vector @ IP = '0': FFF0 0000 Vector set at IP = '0' in hardware BR0 set at FE00
CS1#	x32	DRAM (x32) 0000	4 or 16MBytes
CS2#		Expansion Header UUUU	Routed to Expansion Receptacle
CS3#	x32	Control & Status Registers FA40	Byte and/or word accessible.
CS4#	x8	NVRAM or SRAM FA00	0K, 32K, 128K, or 512KBytes Also available at Expansion Receptacle
CS5#		Expansion Header UUUU	Routed to Expansion Receptacle
CS6#	x16 or U	PCMCIA Slot B Chip Select Even Bytes or Chip Select 6 to I/O Header UUUU	1) OP2 in MPC850 PCMCIA Control Register selects mode: L = PCMCIA Slot B enabled H = CS6# to Expansion Header Enabled
CS7#	x16 or U	PCMCIA Slot B Chip Select Odd Bytes or Chip Select 7 to I/O Header UUUU	1) OP2 in MPC850 PCMCIA Control Register selects mode: L = PCMCIA Slot B enabled H = CS7# to I/O Expansion Header Enabled
IMMR	x32	Value at reset = FF00 0000, then set to FA20 0000	

Address maps are recommended values for the RPX Lite, but other mappings can be utilized for any given application.

U = User or Application Defined

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III. BSP Code Location

At start-up, the code for the RPX Lite is always located in the second to highest 512K block of memory. This 512K block of memory is reserved for the BSP or RTOS (FLASH intensive RTOSs will require a larger block of memory).

Table 3: Code Location in x32 FLASH

		FLASH Memory Option			
Address Range	Block Size	2MByte 29LV400	4MBytes 29LV800	8MBytes 29LV160	16MBytes 29LV320
FFFF FFFF - FFF8 0000	512KB	User	User	User	User
FFF7 FFFF - FFF0 0000	512KB	BSP	BSP	BSP	BSP
FFEF FFFF - FFE8 0000	512KB				
FFE7 FFFF - FFE0 0000	512KB				
FFDF FFFF - FFD8 0000	512KB				
FFD7 FFFF - FFD0 0000	512KB				
FFCF FFFF - FFC8 0000	512KB				
FFC7 FFFF - FFC0 0000	512KB				
FFBF FFFF - FFB8 0000	512KB				
FFB7 FFFF - FFB0 0000	512KB				
FFAF FFFF - FFA8 0000	512KB				
FFA7 FFFF - FFA0 0000	512KB				
FF9F FFFF - FF98 0000	512KB				
FF97 FFFF - FF90 0000	512KB				
FF8F FFFF - FF88 0000	512KB				
FF87 FFFF - FF80 0000	512KB				
FF7F FFFF - FF78 0000	512KB				
FF77 FFFF - FF70 0000	512KB				
FF6F FFFF - FF68 0000	512KB				
FF67 FFFF - FF60 0000	512KB				
FF5F FFFF - FF58 0000	512KB				
FF57 FFFF - FF50 0000	512KB				
FF4F FFFF - FF48 0000	512KB				
FF47 FFFF - FF40 0000	512KB				
FF3F FFFF - FF38 0000	512KB				
FF37 FFFF - FF30 0000	512KB				
FF2F FFFF - FF28 0000	512KB				
FF27 FFFF - FF20 0000	512KB				
FF1F FFFF - FF18 0000	512KB				
FF17 FFFF - FF10 0000	512KB				
FF0F FFFF - FF08 0000	512KB				
FF07 FFFF - FF00 0000	512KB				

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1) Reset vector @ FFF0 0100 but for A[0:3 4:7 8:11]:

   A(0:10) = X for 2MBytes
   A(0:9) = X for 4MBytes
   A(0:8) = X for 8MBytes
   A(0:7) = X for 16MBytes

   where X = "don't' care" (i.e. the address lines defined by "X" are not connected to the FLASH memory)

2) The actual on-board FLASH memory size is mirrored throughout the entire address space (excluding internal processor address spaces) until OR0 is written.

3) Flash base address is remapped to FE00 0000 when BR0/OR0 is written.

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IV. Board Status and Control Registers (BSCRs)

There exists on-board control and status registers. These registers are configured as a x32 port and can be accessed via byte, word, or longword. The registers are defined as shown in the Table below. All registers are read modify write capable (except register 3 which is read only).

Upon power-up (HRESET#) the default value configured in the registers, after masking ("anding") with FF 1F F8 FF, is longword 3E 00 80 UU (i.e. if the first access to the BCSR after reset is a longword read, the value read, after masking with FF 1F F8 FF will be 3E 00 80 UU, where UU is as defined below).

Register values at reset (values in binary and "x" = undefined or determined by function):
R/W Register 0 = 0011 1110
R/W Register 1 = xxx0 0000
R/W Register 2 = 1000 0xxx
RO Register 3 = xxxx 11xx (UU = first four bits = dipswitch setting, 1, 1, NVRAM Battery status, RTC Battery Status)

Table 4: BCSR0

Register Number	Byte Address	Function	Bit	Mnemonic	Definition
0 R/W reset value = 0011 1110	FA40 0000	Ethernet XCVR Control	0	ETHEN	0 = Disable Transceiver 1 = Enable Transceiver
			1	ETHLPBK	0 = Disable Transceiver Loop Back Test 1 = Enable Transceiver Loop Back Test
			2	COLTEST#	0 = Enable collision testing on Transceiver 1 = Disable collision testing on Transceiver
			3	FULLDPLX#	0 = Enable full duplex mode of operation 1 = Disable full duplex mode of operation
		LEDS	4	LED4	0 = LED "on" 1 = LED "off"
			5	LED5	
		CS4# Control	6	ENNVRAM	0 = Disable on-board NVRAM and Enable CS4# at I/O Receptacle 1 = Enable on-board NVRAM and Disable CS4# at I/O Receptacle
		Monitor XVCR Control	7	ENMONXCVR	0 = Disable Monitor Port Transceiver 1 = Enable Monitor Port Transceiver

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Table 5: BCSR1

<table>
<tr><th>Register Number</th><th>Byte Address</th><th>Function</th><th>Bit</th><th>Mnemonic</th><th>Definition</th></tr>
<tr><td rowspan="6">1

R/W

reset value
=
xxx0 0000</td><td rowspan="6">FA40
0001</td><td rowspan="3">Unused</td><td>8</td><td colspan="2" rowspan="3">Unused</td></tr>
<tr><td>9</td></tr>
<tr><td>10</td></tr>
<tr><td></td><td>11</td><td>IPB5SEL</td><td>0 = BVD2/SPKR signal routed to IPB5
1 = INPACK#/DREQ signal routed to IPB5</td></tr>
<tr><td rowspan="3">PC
Slot B
Control</td><td>12</td><td>PCVCTL4</td><td rowspan="2">Defines VCC_SLOT voltage on PCMCIA Slot B:

<u>GND +5.0V +3.3V GND</u>
0 0 1 1
0 1 0 1</td></tr>
<tr><td>13</td><td>PCVCTL5</td></tr>
<tr><td>14</td><td>PCVCTL6</td><td rowspan="2">Defines VPP_SLOT voltage on PCMCIA Slot B:

<u>GND Note 1 Note 2 HI-Z</u>
0 0 1 1
0 1 0 1

Note 1: Hi-Z if VCC_SLOT = GND, else +12.0V.
Note 2: Hi-Z if VCC_SLOT = GND, else VCC_SLOT Voltage</td></tr>
<tr><td>15</td><td>PCVCTL7</td></tr>
</table>

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Table 6: BCSR2

Register Number	Byte Address	Function	Bit	Mnemonic	Definition
2 R/W reset value = 1000 0xxx	FA40 0002	USB Control	16	USBSUSP	0 = Enable USB Transceiver 1 = Disable USB Transceiver
			17	USBSPD	0 = Low Speed (6MHZ USB clock) 1 = High Speed (48MHZ USB clock)
			18	USBPWREN	0 = Disable +5.0V power to USB connector 1 = Enable +5.0V power to USB connector - do not enable if 3V power option is used
			19	ENUSBCLK	0 = Disable USB clock to PA5 1 = Enable USB clock to PA5
			20	ENPA5HDR	0 = Disable PA5 at P2 Receptacle 1 = Enable PA5 at P2 Receptacle
		Unused	21	Unused	
			22		
			23		

Note: - The USB clock can be fed to both PA5 and the P2 Receptacle.
- The USB clock is currently set for 6MHZ and 48MHZ. Via special, this "USB Clock" can be set to any realizable frequency as provided for by the on-board CY2071A clock synthesizer.

Table 7: BCSR3

Register Number	Byte Address	Function	Bit	Mnemonic	Definition
3 R only W = xx reset value = xxxx 11xx	FA40 0003	SW	24	D24	D(2427) defines DipSwitch Settings (D24 is MSb, D27 is LSb) (D24 = position 0 on switch)
			25	D25	
			26	D26	
			27	D27	
			28	RPXL	Reserved (reads back '1')
		Flash	29	RDY/BSY#	0 = Flash operation executing and busy 1 = Flash operation complete
		Nvram	30	BWNVR#	0 = NVRAM Battery is low 1 = NVRAM Battery is good or no NVRAM installed
		RTC	31	BWRTC#	0 = Real Time Clock Battery is low or no External Battery is attached 1 = Real Time Clock Battery is good

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V. I2C Devices/Addressing

The board contains two devices on the I2C bus. These two devices are a Serial EEPROM (SEP) and a Serial Temperature & Thermal Monitor (STTM). The I2C bus also routes to the Expansion Header for possible use on Expansion board designs. The I2C interface pin SDA from the processor must be programmed as open drain. The I2C interface pin SCL from the processor does not necessarily have to be programmed as an open drain signal, because presently there are no other master I2C devices that reside on the I2C bus. If a master I2C device where designed onto an expansion card, then the SCL signal must also be programmed for open drain operation. The RPX Lite board sets both I2C signals to open drain operation.

Table 8: I2C Address Map

Device	Function	I2C Addressing
SEP	Configuration Information	A8h - A9h for 1K/2K devices (128/256 x 8) A8h - ABh for 4K device (512 x 8) A8h - AFh for 8K device (1K x 8)
STTM	Serial Temperature and Thermal Monitor	90h - 91h (8 bytes in device)

A. SEP Format/Interface Structure

Data is stored in the EEPROM device as a series of ASCII records. Each record is terminated with the NEWLINE character (ASCII hex 0x0A), and the last record is terminated with two NEWLINE characters.

All data bytes after the double NEWLINE of the last record have the binary value 0xFF.

Each record consists of a name and a value which are separated by an '=' character. A name identifies the meaning of the value which follows it. For example, the record HZ=50 declares the system frequency (in MHZ) to be 50.

For more information on the names used in records, please read the section or appendix on EEPROM data formats in the RPX Utility Software Manual.

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B. STTM Format/Interface Structure

The driver for the STTM sets the interrupt out for low true operation. Interrupt mode is selected but is not enabled at the processor (IRQ1#). The driver returns the temperature of the device and also a calibrated temperature for reporting ambient air temperature. The calibration parameter is programmed into the SEP and is used to extrapolate ambient air temperature.

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C. System Integration Timers

Table 9: TBSCR, RTCSC, and PISCR

Mnemonic	Internal Address	Value = Bits 0-15 Default Value	Function
TBSCR	200	VVC3 00C3	VV = User Specified Interrupt Level Time Base and Decrementer Enabled but Stopped on FRZ
RTCSC	220	VVC1 00C1	VV = User Specified Interrupt Level RTC Enabled but not stopped on FRZ
PISCR	240	VV83 0083	VV = User Specified Interrupt Level Periodic Timer Enabled, but Stopped on FRZ and Periodic Timer Interrupt Disable

Note: These registers powered by the KAPWR pin (Battery Backed Circuits). They will only be reset on POR (when battery voltage is not available or applied for the first time, and the system powers up). The RPX Lite requires an external battery for back-up operation.

D. PCMCIA Control Registers

PCMCIA port A is not implemented on the MPC823 or MPC850 family.

Table 10: PGCRA and PGCRB

Mnemonic	Internal Address	Value - Bits 0-15 Default Value	Function
PGCRA	0E0	Reserved - not implemented in the MPC850/MPC823	
PGCRB	0E4	VVLL 0080 0000 0080	VV = User Specified Interrupt Level for PCMCIA Card LL = User Specified Interrupt Level for Status Change Internal DMA request disabled Buffers for Card B disabled (OP2 deasserted) and CS6#/CS7# valid at I/O Header Reset signal active (OP3 asserted)

Note: OP2 in PGCRB has a dual function in that it either enables the buffers for PCMCIA Slot B or enables the buffers which allow the CS6# and CS7# signals to be active at the I/O Header:
(If Bit 24 = CBOE = 0 then PCMCIA Slot B Buffers Enabled and CS6#/CS7# not active at I/O Header)
(If Bit 24 = CBOE = 1 then PCMCIA Slot B Buffers Disabled and CS6#/CS7# active at I/O Header)

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E. Option Register Mask Table

Table 11: OR Mask

A(0:12) in OR's	"mmmm m" in Table above
F800 0	128MBytes
FC00 0	64MBytes
FE00 0	32MBytes
FF00 0	16MBytes
FF80 0	8MBytes
FFC0 0	4MBytes
FFE0 0	2MBytes
FFF0 0	1MByte
FFF8 0	512KBytes
FFFC 0	256KBytes
FFFE 0	128KBytes
FFFF 0	64KBytes
FFFF 8	32KBytes

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VI. Interrupt Structure

Table 12: Interrupt Structure for the RPX Lite

Entity	Interrupt	Code	Function
External Interrupt	IRQ0#	00	Power Fail
	IRQ1#	08	Temperature and Thermal Monitor (STTM)
	IRQ2#	10	
	IRQ3#	18	Availability depends on configuration - On I/O Header (pin multiplexes IRQ3# with DPAR0)
	IRQ4#	20	Availability depends on configuration - On I/O Header (pin multiplexes IRQ4# with DPAR1)
	IRQ5#	28	Availability depends on configuration - On I/O Header (pin multiplexes IRQ5# with DPAR2)
	IRQ6#	30	Availability depends on configuration - On I/O Header (pin multiplexes IRQ6# with DPAR3)
	IRQ7#	38	From Header
	NMI		From Watchdog Timer or IRQ0#
Internal	Level 0	04	Routing from interrupt sources below. Actual routings depended on application
	Level 1	0C	
	Level 2	14	
	Level 3	1C	
	Level 4	24	
	Level 5	2C	
	Level 6	34	
	Level 7	3C	
SIU	DEC		Each source is software routed to any "Level" (Each source has unique "vector")
	TB		
	PIT		
	RTC		
	PCMCIA		
CPM	Port C Pins		32 sources combined into one interrupt which is software routed to any "Level" (Each source has unique "vector")
	SCC(1:4)		
	Timer(1:4)		
	DMA		
	RISC Timer		
	I2C		
	SPI		
	SMC1		
	SMC2		
	USB		

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VII. Processor Pin Assignments

The following sections define the function that is associated with certain processor pins. Many of the processor pins have multiple functions, most of which are programmable by the FW. This section will detail the functionality associated with the respective processor pins, and must be used by the firmware/software to correctly configure the system.

A. Bus Interface Pins

Table 13: Bus Interface - Multiple Function Pins

Processor Pin Name	Defined Function	Additional comments	At Expansion Socket
SIZ0/REG#	SIZ0 and REG#		Y
BDIP/GPLB5[1]	BDIP#	Unused	Y
RSV#/IRQ2#[1]	IRQ2#	Unused	Y
KR#/RETRY#/IRQ4#/SPKROUT[1]	RETRY#	Unused	Y
DP0/IRQ3#[1]	IRQ(3:6)#	Can be redefined for DP(0:3) for an Expansion Card that requires Parity. Use IRQ7# or one of the Port C pins for interrupt capability	Y
DP1/IRQ4#[1]			
DP2/IRQ5#[1]			
DP3/IRQ6#[1]			
FRZ/IRQ6#[1]	FRZ		N
CS6#/CE1B#	CS6# or CE1B#	See OP2 below	Y
CS7#/CE2B#	CS7# or CE2B#	See OP2 below	Y
GPLA0#		UPM Output Enable	Y
GPLA1#		GPCM Output Enable	Y
GPLA2#/CS2#[1]	GPLA2#	Only used at I/O Expansion Socket	Y
GPLA3#		Unused	Y
UPWAITA/GPLA4#[2]	UPWAITA	Unused, Pulled-Down	N
UPWAITB/GPLB4#[2]	UPWAITB	Unused, Pulled-Down	N
GPLA5#		Unused	Y
ALEB/DSCK/AT1[3]	ALEB	PCMCIA Slot B ALE signal	N
OP2/MODCK1/STS#[3]	OP2	PCMCIA Slot B Buffer Enable 0 = Enable Buffers, Disable CS6#/CS7# at I/O Header 1 = Disable Buffers, Enable CS6#/CS7# at I/O Header (MODCK1 @ reset rising = '0')	N
OP3/MODCK2/DSDO[3]	OP3	PCMCIA Slot B Reset Signal (MODCK2 @ reset rising = '0')	N

[1] Programmed in SIUMCR

[2] Programmed in MAMR

[3] Hard Reset Configuration and SIUMCR

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B. PCMCIA Interface Pins

The hard reset word configures the following pins to function as PCMCIA signals.

Table 14: PCMCIA - Multiple Function Pins

Processor Pin Name	PCMCIA Function	Additional comments	At Expansion Socket
IPB0	VS1		No
IPB1	VS2		
IPB2	WP or IOCS16# or DREQ#	Function depends on memory or I/O Card	
IPB3	CD2		
IPB4	CD1		
IPB5	BVD1 or SPKR or DREQ#	Function depends on memory or I/O Card (see Note 1)	
IPB6	BVD2 or STSCHG	Function depends on memory or I/O Card	
IPB7	RDY or IRQ#	Function depends on memory or I/O Card	
WAITB#	Wait States		
OP3	Reset Signal		
OP2	Buffer Enable/Disable Control & CS6#/CS7# Enable/Disable Control	Used to enable or disable the on-board buffers that isolate the PCMCIA bus from the Processor bus. In addition, this signal also enables or disables chip selects 6 and 7 from the I/O Header. When the Buffers are enabled, CS6# and CS7# are disabled. When the Buffers are disabled, CS6# and CS7# are enabled.	

Note 1: The PCMCIA signal INPACK# is not required by the MPC8XX, and as such, not supported. Some PCMCIA type DMA cards route the DREQ signal on the INPACK# pin. To support these cards, Control Register 2, bit 19, allows routing of the INPACK# (DREQ) signal to IPB5.

Note 2: BCSR1, bits 12-15, also controls the operation of the PCMCIA interface (voltages to socket).

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C. I/O Port Interface Pins

Refer to the pinouts document for pinout assignments.

3) Any of the port signals that are used for on-board functions can be used on an Expansion Card if the respective on-board function is disabled (via the BCSRs).

4) Port C pins can also be defined as interrupt signals to the processor core. Each Port C pin that is configured as an interrupt pin has a unique vector associated with it, and each pin can be defined as edge or low level active. This allows Expansion Cards to use Port C pins as interrupt lines to the processor if needed. Check the P1_P2.xls spreadsheet for available Port C pins and also see note 3) above.

5) The I2C bus (PB26 and PB27 pins) is used on-board but also routed to the I/O Header. See the I2C section above for used I2C addresses.

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VIII. Performance

See "Clocks and Reset Registers" section for the exact frequency that processor is running at.

A. @ 20 or 25MHZ

Single Beat Read	3 clocks (1 wait states)
Single Beat Write	2 clocks (0 wait states)
Burst Read	7 clocks (1:1:2:1 cycle)
Burst Write	5 clocks (0:1:1:1 cycle)
Refresh	2 clocks

Back to Back Accesses, including refresh, have 1 clock between accesses

B. @ 33MHZ

Single Beat Read	3 clocks (1 wait states)
Single Beat Write	3 clocks (1 wait states)
Burst Read	9 clocks (1:2:2:2 cycle)
Burst Write	5 clocks (0:1:1:1 cycle)
Refresh	3 clocks

Back to Back Accesses, including refresh, have 1 clock between accesses

C. @ 40MHZ

Single Beat Read	4 clocks (2 wait states)
Single Beat Write	4 clocks (2 wait states)
Burst Read	10 clocks (2:2:2:2 cycle)
Burst Write	10 clocks (2:2:2:2 cycle)
Refresh	4 clocks

Back to Back Accesses, including refresh, have 1 clock between accesses

D. @ 50MHZ

Single Beat Read	5 clocks (3 wait states)
Single Beat Write	5 clocks (3 wait states)
Burst Read	11 clocks (3:2:2:2 cycle)
Burst Write	10 clocks (3:2:2:1 cycle)
Refresh	5 clocks

Back to Back Accesses, including refresh, have 1 clock between accesses

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E. @ 66MHZ

Single Beat Read	6 clocks (2 wait states)
Single Beat Write	6 clocks (2 wait states)
Burst Read	18 clocks (2:4:4:4 cycle)
Burst Write	10 clocks (1:2:2:2 cycle)
Refresh	6 clocks

Back to Back Accesses, including refresh, have 2 clocks between accesses

F. @ 81MHZ

Single Beat Read	8 clocks (4 wait states)
Single Beat Write	8 clocks (4 wait states)
Burst Read	20 clocks (4:4:4:4 cycle)
Burst Write	20 clocks (4:4:4:4 cycle)
Refresh	8 clocks

Back to Back Accesses, including refresh, have 2 clocks between accesses